In the Specification

Attached on separate sheet is revised FIG. 2A.

Paragraph 42

During a change in the state of the signals (out) accessible at output 7b of the amplifier circuit from "low logic" to "high logic" (or conversely when the state of the signals "out" change from "high logic" to "low logic") the signal at output 11 of the first inverter 3a changes its state from "high logic" to "low logic"(or conversely, from "low logic" to "high logic"), according to delay times that differ from each other; consequently the output signal (DatoV) accessible at an output 12 of the second inverter 2b, also changes from a "low logic" state to a "high logic" state, or conversely from a "high logic" to a "low logic" state (again according to delay times that differ from each other).

Paragraph 67

~~The~~ To compensate for this effect, a characteristic of the voltage converter shown in Figures 2a and 2b is used (also shown in Figure 3) namely that the delay period d1' occurring at a positive flank of the internal signals (in) on the signal (out) is as long – due to the symmetrical construction of the amplifier circuit 102 – as the delay period d1'' occurring at a negative flank of the internal signals (in) on the complementary signal (bout) (or conversely, that the delay period d2' occurring at a negative flank of the internal signal (in) on the signal (out) is as long as the delay period d2''occurring at a positive flank of the internal signal (in) on the complementary signal (bout)).

Paragraph 68

As shown in detail in Figure 2a, the signal (out) present at the second output 107b of the amplifier circuit 102 of the voltage converter is connected by means of a conductor 109b to an input of the second inverter 103b according to the prototype shown, while the complementary signal (bout) present at the first output 107a of the

amplifier circuit 102 is connected to an input of the first Inverter 103a~~.~~ by means of a conductor 109a.